AMENDMENT

IN THE TITLE:

Please delete the title of the application and change the title to "Dual Damascene Interconnect Structure and Method of Fabrication."

IN THE CLAIMS:

Please amend the claims as follows:

1. (Original) A mask layer overlaying a low-k dielectric material deposited over an underlying metal layer of an integrated circuit device, for use in the construction of an interconnect structure of the integrated circuit device, said mask layer comprising:

a. a passivation mask film deposited on the low-k dielectric material;

b. a barrier mask film deposited over the passivaton mask film; and,

c. a metallic mask film deposited over the barrier mask film.

2. (Original) The mask layer of claim 1 wherein said passivation mask film comprises silicon dioxide or silicon carbonite.

3. (Original) The mask layer of claim 1 wherein said barrier mask film comprises silicon nitride.

4. (Original) The mask layer of claim 1 wherein said metallic mask film comprises a refractory metal or a refractory metal alloy.

5. (Original) The mask layer of claim 4 wherein said refractory metal is chosen from a group of refractory metals comprising titanium, tantalum and tungsten, and said refractory metal alloy is chosen from the group of refractory metal alloys comprising titanium nitride and tantalum nitride.

6. (Currently amended) A method of forming a dual damascene interconnect structure of an integrated circuit device, said interconnect structure having a low-k dielectric material deposited over an underlying metal layer, comprising the steps of:

a. forming a passivation mask film over the low-k dielectric material;

b. forming a barrier mask film over the passivation mask film;

c. forming a metallic mask film over the barrier mask film, and said passivation ~~barrier~~ film and metallic mask films forming a mask layer overlaying said low-k dielectric material;

d. etching a trench within the mask layer, through the metallic mask film, without exposing the low-k dielectric material to a predetermined depth of the low-k dielectric material; ~~and,~~

e. after etching the trench, then etching a via through the mask layer and the low-k dielectric material to the underlying metal layer.

7. (Original) The method of claim 6 wherein said passivation mask film comprises silicon dioxide or silicon ~~carbonite~~ carbide.

8. (Original) The method of claim 8 wherein said barrier mask film comprises silicon nitride.

9. (Original) The method of claim 8 wherein said metallic mask film comprises a refractory metal or a refractory metal alloy

10. (Original) The method of claim 9 wherein said refractory metal is chosen from the group of refractory metals including titanium, tantalum and tungsten, and said refractory metal alloy is chosen from the group of refractory metal alloys comprising titanium nitride and tantalum nitride.

11. (Currently amended) The method of claim 11 further including the step of forming a photoresist layer over the metallic mask film, patterning a trench feature in the photoresist layer, etching a trench through the metal mask film and the barrier mask film to the passivation mask film, before etching the trench or via in the low-k dielectric material.

12. (Currently amended) The method of claim ~~6~~ 11 further including the step of forming a photoresist layer over the low-k dielectric material, and patterning a via feature in the photoresist layer, after etching the trench in the mask layer.

13. (Currently amended) The method of forming an interconnect structure on an integrated circuit device having a low-k dielectric material deposited over an underlying metal layer, and a mask layer deposited on the low-k dielectric material, and said mask layer having a desired etch selectivity with respect to the low-k dielectric material ~~layer~~, the method comprising the step of forming a metallic film as part of the mask layer to increase the etch selectivity of the mask layer with respect to the low-k dielectric material, etching a trench within the mask layer, etching a trench within the mask through the metallic mask film, without exposing the low-k dielectric material, and after etching the trench, then etching a via through the mask layer and the low-k dielectric material to the underlying metal layer.

14. (Original) The method of claim 13 wherein said metallic film comprises a refractory metal or a refractory metal alloy.

15. (Original) The method of claim 14 wherein said refractory metal is chosen from the group of refractory metals including titanium, tantalum and tungsten and said refractory metal alloy is chosen from the group of refractory metal alloys including titanium nitride or tantalum nitride.

16. (Currently amended) The method of claim 13 furthering including the steps of forming a passivation mask film over the low-k dielectric material,

forming a barrier mask film over the passivation mask film and said metallic film is formed over the barrier mask film.

17. (Original) The method of claim 15 wherein said passivation mask film comprises silicon dioxide or silicon ~~carbonite~~ carbide.

18. (Original) The method of claim 15 wherein said barrier mask film comprises silicon nitride.

19. (Original) The method of claim 13 further including the steps of etching a trench within the low-k dielectric material to a predetermined depth of the low-k dielectric material, etching a via through the low-k dielectric material to the underlying metal layer of the low-k dielectric material, and depositing a conductive metal within the via and trench.

20. (Currently amended) The method of claim 19 wherein the conductive metal is deposited on the interconnect structure ~~integrated circuit chip~~ outside of the via and the trench and the method further including the steps of planarizing the integrated circuit chip, and removing said excess conductive metal, the metallic mask ~~layer~~ film and the barrier mask film.

21. (Previously added/currently amended) A method for the fabrication of a semiconductor device including a wafer substrate having a dielectric material

formed over a metallization layer formed over said wafer substrate, comprising the steps of:

a. forming a mask layer over the dielectric material wherein said mask layer includes a ~~barrier~~ passivation film, and said mask layer having a known etch selectivity with respect to the dielectric material;

b. depositing a metallic mask film over the ~~barrier~~ passivation film to increase the etch selectivity of the mask layer and forming a mask layer comprising a composite of the ~~barrier~~ passivation mask film and metallic mask film;

c. patterning a first feature in the mask layer after depositing the metallic mask film;

d. etching the first feature through the metallic mask ~~layer~~ film without exposing the underlying dielectric material ~~and in the dielectric material~~ after patterning the first feature in mask layer; ~~and,~~

e. ~~depositing a conductive metal in the feature~~ patterning a second feature in the mask layer, and said second feature overlapping at least a portion of the first feature;

f. etching the second feature in the dielectric material in accordance with the patterned second feature in the mask layer before removing remaining portions of the passivation mask film and the metallic mask film;

g. transferring the first feature from the mask layer to the underlying dielectric material after etching the second feature in the dielectric material; and

h. depositing a conductive metal in the first feature and in the second feature.

22. (Previously added/currently amended) The method of claim 21 further comprising the step depositing ~~a passivation~~ the barrier mask film over ~~the barrier~~ a passivation mask film forming said mask layer as a composite of the barrier mask film, passivation mask film and metallic film.

23. (Previously added/currently amended) The method of claim 22 wherein said etching step comprises the step of etching the feature in the mask layer through the metallic mask films and down to the ~~barrier~~ passivation mask film, then removing the metallic mask film and ~~passivation~~ barrier mask film after etching the first and second features ~~feature~~ in the dielectric material, and before depositing the conductive metal in the feature.

24. (Previously added/currently amended) The method of claim 21 wherein said step of patterning includes patterning a first feature having predetermined width, and patterning a second feature having a predetermined

width different from the predetermined width of the first feature, and said second feature is aligned with respect to said first feature.

25. (Previously added/currently amended) The method of claim 24 wherein said etching step includes etching the first feature in mask layer through the metallic mask film and to the ~~barrier~~ passivation mask film before patterning the second feature, and ~~then etching second feature to the barrier mask film,~~ then etching the second feature a predetermined depth in the dielectric material, before etching the first feature of the dielectric material to a predetermined depth of the dielectric material spaced above the predetermined depth of the second feature.

26. (Previously added) The mask layer of claim 21 wherein said passivation mask film comprises silicon dioxide or silicon carbonite.

27. (Previously added) The mask layer of claim 21 wherein said barrier mask film comprises silicon nitride.

28. (Previously added) The mask layer of claim 21 wherein said metallic mask film comprises a refractory metal or a refractory metal alloy.

29. (Previously added) The mask layer of claim 28 wherein said refractory metal is chosen from a group of refractory metals comprising titanium,

tantalum and tungsten, and said refractory metal alloy is chosen from the group of refractory metal alloys comprising titanium nitride and tantalum nitride.